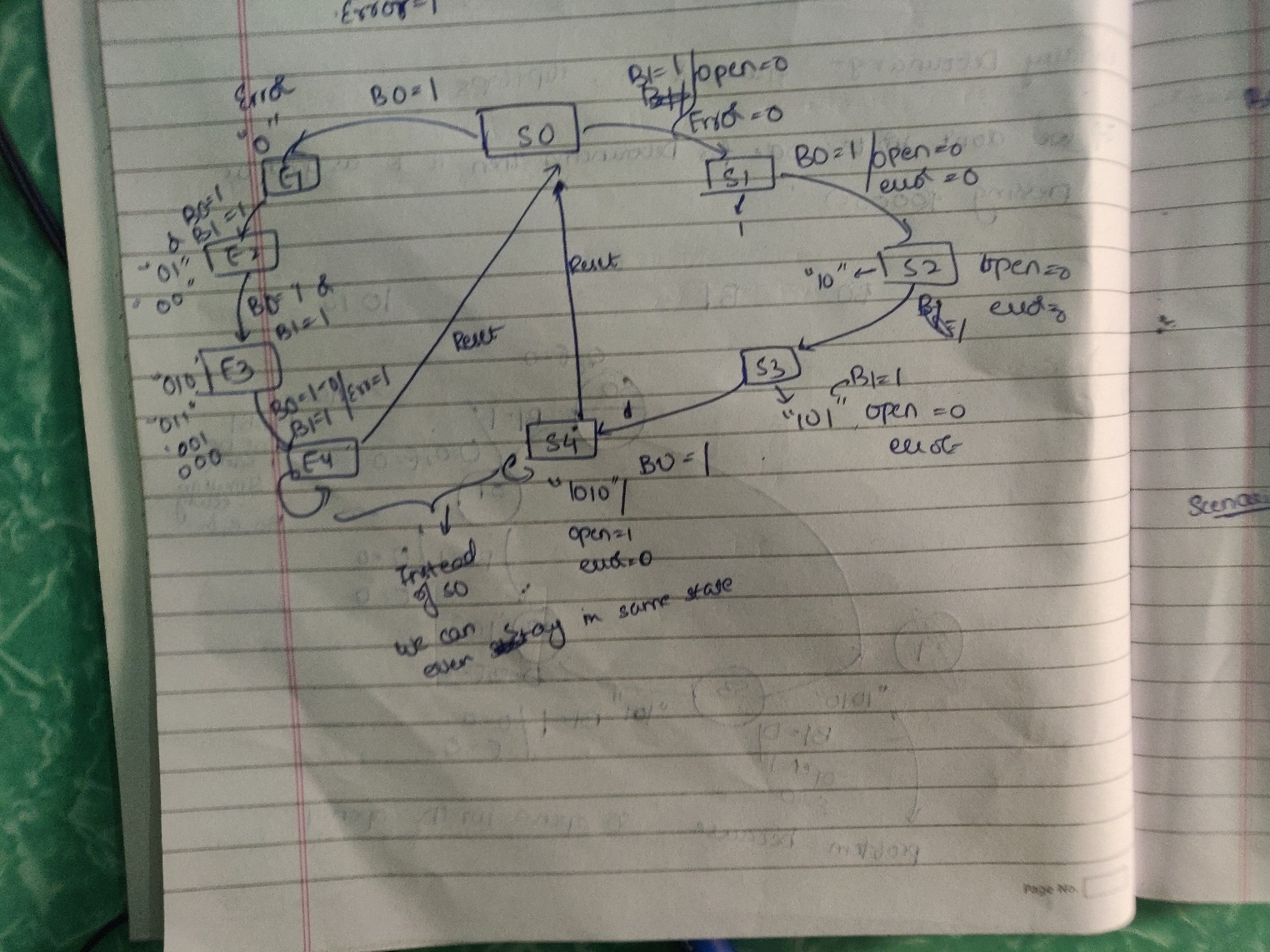
**Lab 7 and 8: Control Unit for Digital Lock-FSM Application**

**Problem Statement:** Design and implement a control unit for a digital lock. The digital lock has the passcode “1010”. The code should be entered via 2 Push Buttons: one button for entering 1’s (use **P16**) and another for entering 0’s (use **R16**). Use a third push button (use **T18**) to add reset functionality. Based on the entered code, glow an LED for the following outputs

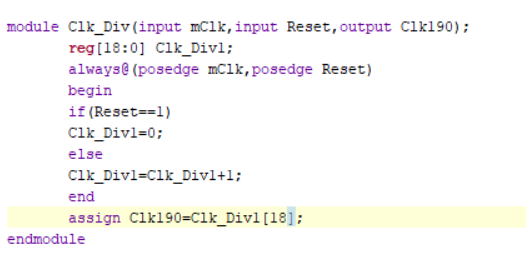
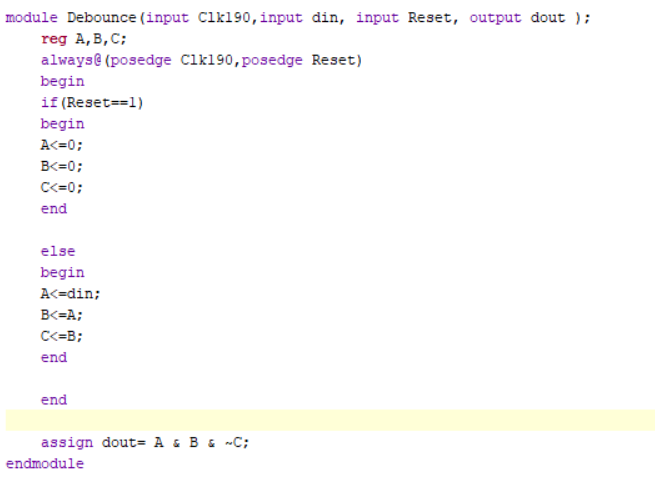
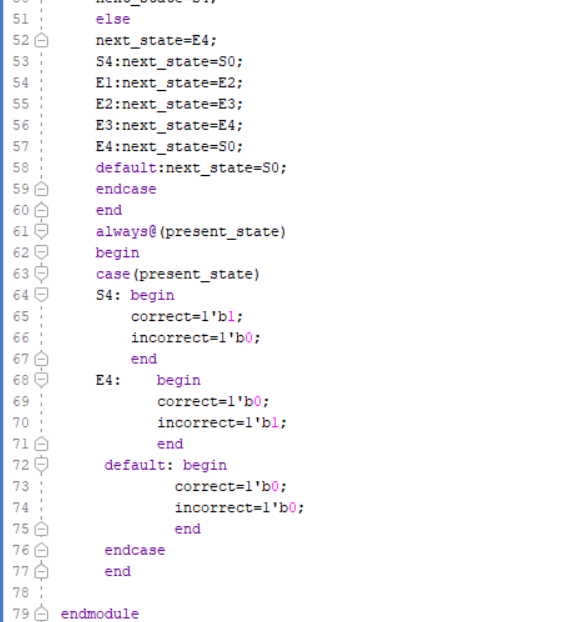
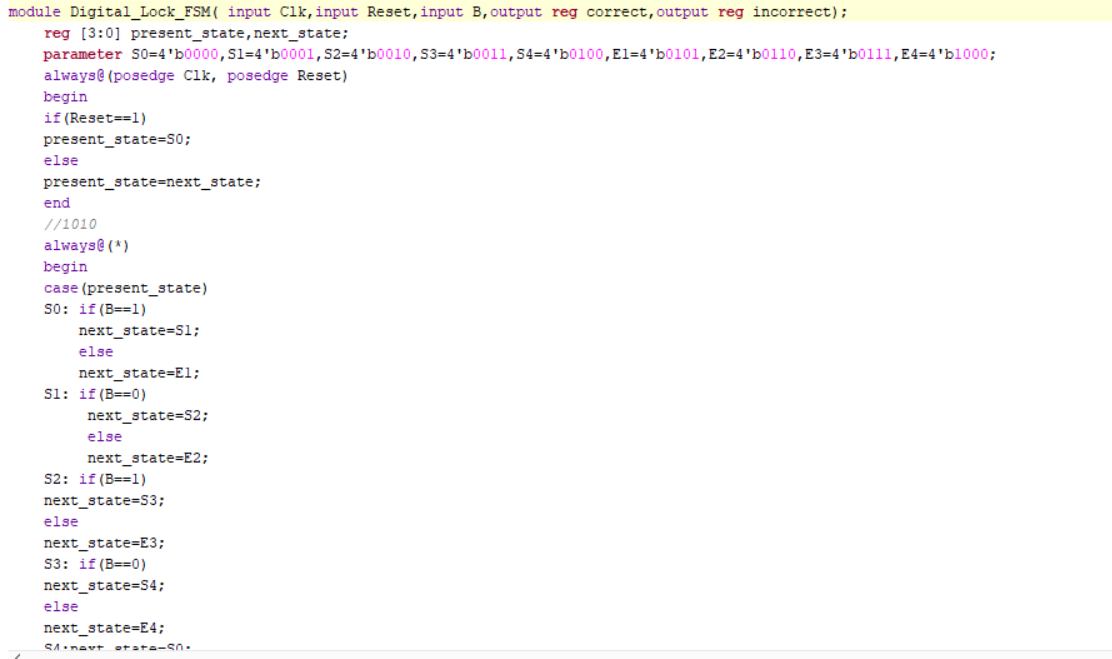
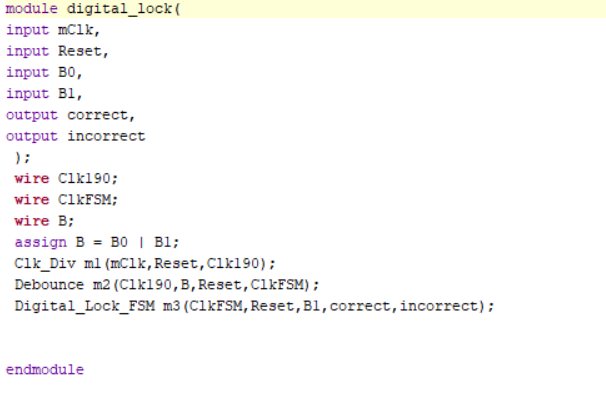
1. LED\_0 (Use pin **T22**) will glow indicating PASS, if the entered 4-digit binary code is correct
2. LED\_1 (Use pin **T21**) will glow indicating FAIL, if the entered 4-digit binary code is incorrect

[Note: Digital debouncing has to be implemented for all push button switches]

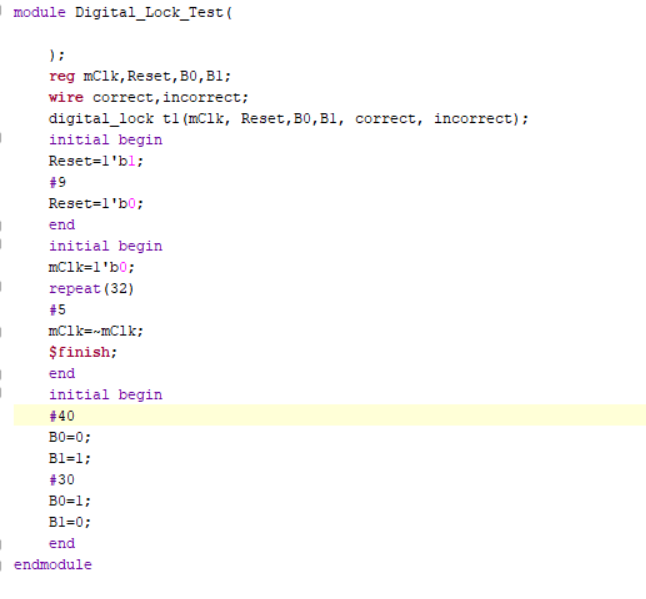
1. **Copy the image of FSM for the above specification (Clearly label all inputs and outputs).**

Answer:

1. **Copy the image of all your Verilog (main and sub modules) Codes below.**

Answer:Clk\_Div (for 200hz/190hz) Debounce: Digital Lock FSM: Final Module: 

1. **Copy the image of Test Bench Verilog code below.**

Answer: 

1. **Implement the design on FPGA after including clock division (Elaborate, I/O Plan, Synthesize, Implement, Bitstream and Program) and verify the outputs. Please use the same pins mentioned above for inputs and outputs.**
2. **Check the output on FPGA.**
3. **Show the output to the instructor.**
4. **Submit All source files (design, Test Bench and Constraints) and Bitstream file in your respective folder.**